VT1682 Programming Note V1.0

2. REVISION HISTORY

Revision	Date	Remark
V1.0	2006/11/09	First edition

3. Problem List

	Function	Description	Solution
1	XIOF	XIOF3 is unable to change to input mode	None
		Mistake when using XIOF0 and XIOF1 as output	It's wired to FPGA on EVB. If the input mode is required, please cut off the wire between FPGA and VT1682
2	ADC	XIOF3 would be in-valid in ADC port.	Using IOE3, please reference the following section 4.1.
		Mistake when using XIOF0 and XIOF1 as ADC port	It's wired to FPGA on EVB. If the ADC mode is required, please cut off these two wires between FPGA and VT1682
3	TV System	Switching TV system would breakdown the game	Please reference the following section 4.2.
4	Divider	Remainder is incorrect	Please reference **6.1.2 Divider** in **Programming Guide**.
5	UART	Status is invalid	Address is changed to $211B
6	DMA	Mistaken when DMA from internal RAM to the external RAM.	There is a limitation on the address when the DMA path was from internal RAM to the external RAM. The target and source byte address A[12] should be the same.
		Mistaken when DMA from internal RAM to internal RAM.	DMA from internal RAM($0000~$1FFF) to internal RAM($0000~$1FFF) is not allowed.
		Bank crossing	DMA bank size is 64Kbytes. DMA address would not be able to cross the bank.
7	PPU-BK2	Graphic mistaken in BK2 256 color mode	None
		Horizontal position two pixels shift	None
8	PPU-Sprite	Sprite horizontal flip function is invalid.	None
9	VRAM	Data in VRAM are unable to be read through the port $2007	None
10	Sprite RAM	Data in VRAM are unable to be read through the port $2004	None

11	Bank register	Ports between $2110~$2113 have different read/write mapping address	Reference the **Register Table** in **Programming Guide**
12	Audio DAC	There are some noises when playing audio.	Prevent from using the MSB of the audio DAC.
13	Sleep mode	The sleeping mode is invalid in VT1682	None
14	CCIR	There are false colors for some high luminance color in YUV mode.	Using the CCIR RGB interface
15	TFT LCD	There are black dots on the screen when the LCD_CLK in $200C is 3	None
16	CSTN LCD	Partial CSTN are unable to display.	For the detail CSTN protocol timing diagram, please contact with VRT FAE.
17	EXT IRQ	Main CPU external IRQ is high level trigger not negative edge trigger.	Using an external 74xx74 or using the SCPU external IRQ(SCPU_UIOB[7]).

4. Illustration demo code for the problem list

4.1 ADC

The ADC port on XIOF3 is invalid, but XIOF0, XIOF1 and XIOF2 are valid. If the forth ADC port is necessary, please change to the AGC port XIOE3 with the modification in your program as shown in the following instruction.

```
// Set the IOE3 to input mode in the initialization
        lda     #$81    // Bit7 : 1 :Switch ADC to IOE3
                        //      : 0 Switch ADC to IOFX
        sta     $211F
        :
        :
        :
        lda     $211E
        eor     #$ff    // a_reg : ADC DATA
```

4.2 TV system configuration

The application for the PAL system requires to switch the register TV_SYS_SEL[1:0] in $2105. The switching operation should be done in the beginning of the RESET program, as shown in the following instruction.

```
RESET:
        lda   #$30
        lda   #$30
        lda   #$30
    if TV_SYSTEM=PAL
        lda   #$30
    else
        lda   #$00
    endif
        sta   $2105
        :
        :
```

Please note that the “$2105.D[5:4] should not be changed after the above instructions.

5. Initialization Note

5.1 Working RAM Initialization

All data in internal RAM ($0000~$1FFF) should be initialized in the beginning of the program. Please note that not all data in every chip has the same power on value. In other word, all data in the RAM would be random value without initialization and un-predictable.

5.2 Sprite RAM initialization

Please note that it's necessary to initialize the Sprite RAM before the graphic (background layer or sprite layer) is enabled. The initialization method is to write 1536 "0" into Sprite Data ($2004), otherwise the display screen would be not predictable.